



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/931,124

08/16/2001

Takahiko Kishi

678-724

3618

66547 7590 10/16/2007
THE FARRELL LAW FIRM, P.C.
333 EARLE OVINGTON BOULEVARD
SUITE 701
UNIONDALE, NY 11553

EXAMINER

ZHENG, EVA Y

ART UNIT

PAPER NUMBER

2611

MAIL DATE

DELIVERY MODE

10/16/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/931,124	Applicant(s) KISHI, TAKAHIKO	
	Examiner Eva Yi Zheng	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-18 is/are allowed.
- 6) ☒ Claim(s) 1-7,9-15 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/6/07 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – (1) Prior art Chalmers's two mixers 132 and 134 in Fig. 1 can not equate to the second mixer in claim 1. (2) It is not obvious to combine the teaching of Yasuda and Chalmers.

Examiner's response – (1) According to current application, the second mixer (205 in Fig. 1) is a quadrature converter, which comprises multiplier and frequency oscillator ([0031]). Prior art Chalmers has shown exactly such quadrature convert in Fig. 1, block 126, 132 and 134. Therefore, Chalmers qualify and meet the claimed limitations. (2) Chalmers disclose all the subject matters except for the specific teaching of a decimation filter. However, Yasuda., disclose a receiver system comprises an analog decimation filter to suppress the signal which may turn out to be aliasing noise (105 in Fig. 3; Col 2, L40-47). It is advantages to implement an analog decimation filter in a receiver, so that noise and unwanted signals are removed, and the quality of signal is improved. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of analog decimation filter of Yasuda with the receiver system of Chalmers.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view of Yasuda (US 6,181,740), further in view of Poklemba (US 5,696,796).

a) Regarding to claim 1, Chalmers disclose a digital down-converter for converting a frequency of a signal, received at a radio receiver and sampled with a radio frequency (RF) or an intermediate frequency (IF), to a detection frequency for a detection process, comprising:

a first mixer (106 in Fig. 1) for converting and outputting a frequency of the received signal to a frequency of a first IF signal by multiplying the signal by a real signal (since the current application is direct to local oscillator DDS 202, Chalmers's local oscillator has the same functionality as the current application) ; and

a second mixer for converting the frequency of the first IF signal having only wanted components outputted by the decimation filter to a second IF signal of the detection frequency, and outputting the second IF signal as a complex signal by multiplying the output of the decimation filter by a complex local signal by multiplying the output of the decimation filter by a complex local signal (126 and output of 132,134 as shown in Fig. 1).

Chalmers disclose all the subject matters described above except for the specific teaching of (1) a decimation filter and (2) a digital signal down converter; a first selector and a second selector.

However, (1) Yasuda., in the same field of endeavor, disclose a receiver system comprises an analog decimation filter to suppress the signal which may turn out to be aliasing noise (105 in Fig. 3; Col 2, L40-47). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of analog decimation filter of Yasuda with the receiver system of Chalmers. By doing so, remove unwanted or undesired signal in a radio receiver system.

(2) Moreover, Poklemba, disclose a digital down converting system comprises A/D converter (204) output to a digital down converter (as shown in Fig. 6). And a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal (206 and 208); and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal (206 and 210; Col 5, L51-59; Though Poklemba does not explicitly describe two selectors, Poklemba sequentially selects from cosine (+1,0,-1,0) and sine (0,+Q,0,-Q) values (Fig. 4 and 6). The current application also sequentially selects from values of 1,0,-1,0 and 0,1,0,-1. Therefore, Poklemba implicitly teaches two selectors.). Therefore, it is obvious to one of ordinary skill in art to implement the sampling method of Poklemba in the receiver system of Chalmers and Yasuda. By doing so, provide no phase imbalance, I/Q crosstalk, and DC offsets in a digital downconverting system. In addition, the quadrature translation can be implemented through multiplication by cosines and sines whose sample values

Art Unit: 2611

are (+1,0,-1,0) and (0,-1,0,-1), respectively (Col 1, L55-59). Therefore, to reduce circuitry complexity.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view of Poklemba (US 5,696,796).

a) Regarding to claim 5, Chalmers disclose a receiver comprising:

a digital down-converter including a first mixer (106 in Fig. 1) for converting a frequency of the received signal, sampled with a radio frequency (RF) or an intermediate frequency (IF), to a frequency of a first IF signal by multiplying the signal by a real signal (120), and a second mixer (112 in Fig. 1) for converting the first IF signal converted by the first mixer to a second IF signal of the detection frequency for a detection process and then outputting the second IF signal as a complex signal by multiplying the first IF signal by a complex local signal (126 and output of 132,134 as shown in Fig. 1).

an RF unit (received signal as shown in Fig. 1) for receiving an input signal and providing the received signal to the digital down-converter for frequency conversion.

Chalmers disclose all the subject matters described above except for the specific teaching of the RF unit output to a third mixer; a filter for attenuating an aliasing frequency component and an image frequency component of the first mixer in the digital down-converter, from an output of the third mixer; an analog-to-digital converter for sampling an output of the filter with a radio frequency or an intermediate frequency and

providing the sampled signal to the digital down-converter; and a first selector and a second selector in the second mixer.

However, Poklemba, disclose a digital down converting system comprises IF signal output to an anti-aliasing filter (202), A/D converter (204), and a digital down converter (as shown in Fig. 6). It is well known and common knowledge to implement a mixer for RF signal converting to IF signal. Thus, a third mixer (input to filter 202) is inherently taught. In addition, Poklemba disclose a first selector for cyclically selecting a multiplication value among cosine wave values of the local signal (206 and 208); and a second selector for cyclically selecting a multiplication value among sine wave values of the local signal (206 and 210; Col 5, L51-59). Though Poklemba does not explicitly describe two selectors, Poklemba sequentially selects from cosine (+1,0,-1,0) and sine (0,+Q,0,-Q) values (Fig. 4 and 6). The current application also sequentially selects from values of 1,0,-1,0 and 0,1,0,-1. Therefore, Poklemba implicitly teaches two selectors. Therefore, it is obvious to one of ordinary skill in art to implement the sampling method of Poklemba in the receiver system of Chalmers. By doing so, provide no phase imbalance, I/Q crosstalk, and DC offsets in a digital downconverting system. In addition, the quadrature translation can be implemented through multiplication by cosines and sines whose sample values are (+1,0,-1,0) and (0,-1,0,-1), respectively (Col 1, L55-59). Therefore, to reduce circuitry complexity.

5. Claims 2-4 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view of Yasuda (US 6,181,740), further in view of Poklemba (US 5,696,796), and in further view of Ostman (US 6,061,385).

a) Regarding to claim 2, Chalmers, Yasuda, and Poklemba disclose all of the subject matter described above except for the specific teaching of a frequency of the first IF signal is $\frac{1}{4}$ a sampling frequency.

Ostman, in same field of endeavor, teaches a received frequency modulated signal as shown in Fig. 1, where the intermediated frequency is a quarter of the sampling frequency (Col 4, L28-36).

To avoid complexity and extreme power consumption of the circuitry a well known method is to select the intermediate frequency to be a quarter of the sampling frequency (Ostman, Col 4, L28-35). Therefore, it is obvious to one of ordinary skill in the art to implement quarter sampling method taught by Ostman in the frequency down conversion system by Chalmers. By doing so, provide simpler digital down converter design and more desirable result. Additionally, reduce power consumption, reduce cost, and simplify communication system design.

b) Regarding to claims 3 and 11, Chalmers discloses further comprising an automatic gain control (AGC) amplifier (110 in Fig. 1) for amplifying of the output of the first mixer and inputting the amplified output to the cosine part and the sine part of the second mixer, and

wherein the first and second selectors are connected to the output of the AGC (Chalmers in view of Poklemba).

c) Regarding to claims 4 and 9, Chalmers discloses the digital down-converter, wherein the second mixer further comprises a multiplier for multiplying the output of the decimation filter by a certain ratio of a sampling frequency and a decoding means for decoding the multiplied signal through the multiplier (as shown in Fig. 1).

d) Regarding to claim 10, the digital down-converter further comprises: wherein the first and second selectors are connected to the output of the decimation filter (Yasuda, and Poklemba).

e) Regarding to claims 12 and 13, Poklemba disclose wherein the first selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value 1, outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0' (106 and 108 in Fig. 4; Col 5, L51-59).

f) Regarding to claims 14 and 15, Poklemba disclose wherein the second selector has multiplication values among cosine wave values as 1, 0, -1 and 0, outputs a multiplication result corresponding to a multiplication value 1, outputs a multiplication result corresponding to '-1' by inversion, and a multiplication result '0' corresponding to a multiplication value '0' (106 and 108 in Fig. 4; Col 5, L51-59).

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US 5,375,146) in view Poklemba (US 5,696,796), and in further view of Ostman (US 6,061,385).

a) Regarding to claim 6, Chalmers and Poklemba disclose all of the subject matter described above except for the specific teaching of a frequency of the first IF signal is $\frac{1}{4}$ a sampling frequency.

Ostman, in same field of endeavor, teaches a received frequency modulated signal as shown in Fig. 1, where the intermediated frequency is a quarter of the sampling frequency (Col 4, L28-36).

To avoid complexity and extreme power consumption of the circuitry a well known method is to select the intermediate frequency to be a quarter of the sampling frequency (Ostman, Col 4, L28-35). Therefore, it is obvious to one of ordinary skill in the art to implement quarter sampling method taught by Ostman in the frequency down conversion system by Chalmers. By doing so, provide simpler digital down converter design and more desirable result. Additionally, reduce power consumption, reduce cost, and simplify communication system design.

b) Regarding to claim 7, Chalmers discloses further comprising an automatic gain control (AGC) amplifier (110 in Fig. 1) for amplifying of the output of the first mixer and inputting the amplified output to the cosine part and the sine part of the second mixer, and

wherein the first and second selectors are connected to the output of the AGC (Chalmers in view of Poklemba).

Allowable Subject Matter

7. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 16-18 are allowed.

9. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches or suggests a digital down-converter as the current application. In specific, a radio receiver for comprises a first mixer for converting signal to a first IF signal and a second mixer for converting to a second IF signal; wherein the second mixer comprises a selector for selecting and inverting signals from two decimation filters for suppressing an unwanted signal of respectively inputted signals.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

Application/Control Number: 09/931,124

Page 12

Art Unit: 2611

you have questions on access to the Private PAIR system, contact the Electronic
Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng
Examiner
Art Unit 2611

October 10, 2007

A handwritten signature in black ink, appearing to read "Chieh M. Fan", with a stylized flourish at the end.

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER